Claims

1. A current folding cell comprising a plurality of current inputs for receiving at least two distinct input currents to be folded, further comprising:

at least one current output,

a plurality of current paths between said current inputs and said at least one current output, each path comprising at least one element,

wherein the current path taken by each input current depends on the sign and/or on the magnitude of said input current,

wherein for at least one input current, when it changes from a first current path to a second current path, and therefore from at least one element to at least one other element, these two or more elements continue to conduct a non-zero current during the complete change of current path.

2. The current folding cell of claim 1, wherein for at least two input currents, when they change from a first current path to a second current path, and therefore from at least one element to at least one other element, these two or more elements continue to conduct a non-zero current during the complete change of current path.

3. The current folding cell of claim 1, comprising at least two current outputs.

4. The current folding cell of claim 2, comprising two current inputs, two current outputs and one current path between each current input and each current output, wherein one current input receives an input current while the second current input receives the same input current with the opposite sign.

5. The current folding cell of claim 4, wherein one current output delivers an output current while the second current output delivers the same output current with the opposite sign.

6. The current folding cell of claim 2, wherein said element is a non-linear element.

7. The current folding cell of claim 2, further comprising comparison means yielding at least one digital output representative of the sign and/or magnitude of said input current or input currents.

8. The current folding cell of claim 4, further comprising at least one current summing circuit where more than one current arrives, the output of said current summing circuit being connected to one of said current inputs.

9. The current folding cell claim 1, comprising a first current input and a second current input,

a first circuit providing two alternate current paths for the first input current,

a second circuit providing two alternate current paths for the second input current,

each of said current paths comprising at least one of said elements,

a first current summing circuit for adding the current from one of the current paths of said first circuit with the current from one of the current paths of said second circuit and for providing the result of the addition to said first current output,

a second current summing circuit for adding the current from the other current path of said first circuit with the current from the other current path of said second circuit, the output of said second current summing circuit being connected to said second current output and for providing the result of the addition to said second current output.

10. The current folding cell of claim 9, wherein the input current in said first circuit is equal in magnitude and opposite in sign to the input current in said second circuit.

11. The current folding cell of claim 10, further comprising first comparison means yielding one digital output indicating the path taken by said current in said first

circuit, and second comparison means yielding a second digital output indicating the path taken by said current in said second circuit.

12. The current folding cell of claim 11, the output of one of said comparison means being used for testing said current folding cell.

13. The current folding cell of claim 4, further comprising first comparison means yielding one digital output indicating the path taken by said current, said comparison means comprising a multi-level comparator yielding a plurality of bits representative of the sign and/or amplitude of at least one of said input currents.

14. The current folding cell of claim 6, wherein at least one of said non-linear elements is constituted by a diode or by a diode-connected transistor.

15. The current folding cell of claim 6, wherein at least one of said non-linear elements is constituted by a transistor.

16. The current folding cell of claim 1, further comprising a biasing circuit for biasing said elements in each path with a bias current sufficiently high compared to the input currents to have two elements conduct when a small non-zero input current is presented to said current input.

17. The current folding cell of claim 16, wherein different biases are applied to said elements in two circuits in the cell.

18. The current folding cell of claim 1, further comprising at least one clipping circuit for limiting the range of said at least one of input current, thus allowing the folding cell to have a larger input current range than without clipping.

19. The current folding cell of claim 18, comprising a plurality of current outputs and further comprising a means to add the output currents of the current folding

cell to the output currents of the clipping circuit in such a way that the sign and/or magnitude of the input currents determines to which output terminal each of the input currents are transferred.

20. The current folding cell of claim 1, wherein at least one of said outputs is used in a feedback loop to control at least one of said inputs in order to obtain negative dynamic resistance in some part of the range of input currents.

21. A circuit comprising at least one folding cell of one of the claims 1 to 20.

22. Circuit of claim 21, wherein said circuit comprises a plurality of current folding cells connected in cascade.

23. The circuit of claim 22, wherein at least one of said outputs of at least one folding cell in the cascade is used in a feedback loop to control at least one of said inputs of at least one folding cell the cascade.

24. The circuit of claim 22, further comprising at least one amplification stage between two cascaded folding cells.

25. The circuit of claim 24, wherein said amplification stage includes a current mirror to amplify the current flowing from one stage to the next one.

26. The circuit of claim 21, wherein the bias current applied to the most significant cells in the cascade is such that the DC-current in the elements in each path is higher than what would be needed to reach the precision of current detection of the least significant stage or stages.

27. The circuit of claim 26, wherein said circuit comprises a plurality of current folding cells operating in parallel on signals of same significance.

28. The circuit of claim 21, wherein said circuit comprises a plurality of cascades of current folding cells operating in parallel on signals of same significance.

29. The circuit of claim 21, further comprising at least one re-injection circuit for reducing the influence of a parasitic capacitance linked to a node by re-injecting in a node a current equal to the capacitive current, but with an opposite sign.

30. The circuit of claim 29, wherein said re-injection circuit re-injects said current into a different node along the current path.

31. The circuit of claim 21, being an analog-to-digital converter.

32. The circuit of claim 31, comprising a plurality of cascades of current folding cells , wherein at least one bit of the digital output of the converter is derived from a plurality of outputs provided by folding cells of the same order or significance in different cascades.

33. The circuit of claim 32, wherein a different offset current is added to the input currents of the different cascades, and wherein the least significant bit(s) is/are determined by establishing the cascade of which the output currents of the last stage were nearest to the zero crossing.

34. The circuit of claim 32, wherein said outputs are current outputs, and wherein output currents provided by folding cells of the same order in different cascades are summed, the result of said sum being used for determining said one bit.

35. The circuit of claim 32, wherein a majority voting scheme is used for deriving said one bit from a plurality of output currents provided by folding cells of the same order in different cascades.

36. The circuit of claim 32, wherein said one bit is derived from a plurality of output currents provided by one or several selected folding cells of the same order in different cascades, wherein only the folding cells corresponding to the cascade or cascades of which the current outputs are nearer to the zero crossing are selected.

37. The circuit of claim 28, further comprising mismatch compensating means for reducing the undesired mismatch between folding cells in different cascades or between the input signals of said cascades.

38. The circuit of claim 37, wherein said mismatch compensating means comprise means for comparing the output currents of each of said cascades and feed-back means for adjusting the mismatch in said cascades depending on the result of the comparison.

39. The circuit of claim 38, wherein said mismatch compensating means comprise a load after a stage in said cascade, said comparison means comparing the voltage loss over said load with a reference, the current after said load being fed back in order to adjust said mismatch.

40. The circuit of claim 22, further comprising a track and hold circuit or sample and hold circuit between at least some stages in the cascade of folding cells to construct a pipelined analog-to-digital converter.

41. The circuit of claim 22, further comprising means for measuring the output current of the last folding cell in said folding cell.

42. The circuit of claim 21, being a mixer for mixing several currents, said mixer comprising a at least one current summing circuit where more than one current arrives, the output of said current summing circuit being connected to one of said current inputs.

43. The circuit of claim 21, being a multilevel memory in which an output current of at least one of said folding cell is used in a feedback loop which controls one or more input of the circuit.

44. The circuit of claim 21, being an array of cells in which said current folding cell are used for providing multi-level detection of the currents in the cells.

45. The circuit of claim 21, being a self-latching analog-to-digital converter in which the current of at least one of said folding cell is used in a feedback loop which controls one or more input of the circuit.

46. The circuit of claim 21, being an oscillator using the change in slopes of the output currents as a function of the input currents, provided by the folding cell.

47. The circuit of claim 22, being used to implement a frequency multiplier.

48. The circuit of claim 21, being used to provide switching means.

49. The circuit of claim 21, further comprising:
level detection means for detecting the level of each of said output,
verification means for verifying the relationship between said levels,
feed-back means for correcting this relationship by acting on said circuit and/or on the input signal of said circuit.

50. The circuit of claim 49, wherein said outputs are current outputs.

51. The circuit of claim 50, wherein said level detection means comprise:
a load after said output, .
and comparing means for comparing the voltage loss over said load to a reference.

52. The circuit of claim 51, wherein said level detection means comprise a load after said output, wherein said verification and feed-back means make use of the current after said load which is fed back into said circuit in order to adjust said relationship.

53. The circuit of claim 21, further comprising at least one current sample-and-hold or track-and-hold circuit,

54. The circuit of claim 53, wherein an input current of said current sample-and-hold or track-and-hold circuit is injected into a terminal of a component or circuit to convert the input current to a voltage so that this voltage can be stored on a storage capacitor, and where the input current is transferred to another terminal of this component or circuit from where it is provided to one folding cell.

55. A current sample-and-hold or track-and-hold circuit, wherein an input current is injected into a terminal of a component or circuit to convert the input current to a voltage so that this voltage can be stored on a storage capacitor, and where the input current is transferred to another terminal of this component or circuit from where it is made available for further use.

56. The current sample-and-hold or track-and-hold circuit of claim 55, where said component or circuit is a transistor.

57. The current sample-and-hold or track-and-hold circuit of claim 56, where said component or circuit is a transconductor.

58. The current sample-and-hold or track-and-hold circuit of claim 55, said output being cascade-connected to the input of another current sample-and-hold or track-and-hold circuit.

59. The current sample-and-hold or track-and-hold circuit of claim 58, the storage nodes of said current sample-and-hold or track-and-hold circuits being mutually capacitively coupled.

60. The current sample-and-hold or track-and-hold circuit of claim 55, wherein an isolation of the storage capacitor during hold mode is provided by means of a circuit acting solely on the source or emitter of one or more transistors.